



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/534,728

12/02/2005

Yukio Sakashita

123887

7173

25944 7590 02/22/2008

OLIFF & BERRIDGE, PLC
P.O. BOX 320850
ALEXANDRIA, VA 22320-4850

EXAMINER

THOMAS, ERIC W

ART UNIT

PAPER NUMBER

2831

MAIL DATE

DELIVERY MODE

02/22/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.		Applicant(s)	
	10/534,728		SAKASHITA ET AL.	
	Examiner		Art Unit	
	Eric Thomas		2831	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 January 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) 3, 6-8, 10 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4, 5, 9 and 11-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on _____ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>12/06</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of species AC in the reply filed on 1/11/08 is acknowledged. The traversal is on the ground(s) that the search and examination of the entire application could be made without serious burden. This is not found persuasive because it would be a serious burden on the examiner to search species of different limitations (different search strategies, reference considerations).

The requirement is still deemed proper and is therefore made FINAL.

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

2. Claim 1 is objected to because of the following informalities:

Claim 1, line 2, delete "for reducing power source noise".

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

Art Unit: 2831

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-2, 4-5, 11,13 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP 2001-326305 ('305) in view of Takayuki (JP 08-253324).

'305 discloses a thin film capacitor for reducing power noise connected to a power source wherein the capacitor has a dielectric film (see paragraph 6 - ferroelectric film).

'305 discloses the claimed invention except for the dielectric film being formed with a bismuth layer structured compound wherein the c axis is oriented substantially vertically with respect to the plane of a thin film forming substrate, and said bismuth layer structured compound is expressed by the following formula $(\text{Bi}_2\text{O}_2)^{2+}(\text{A}_{m-1}\text{B}_m\text{O}_{3m+3})^{2-}$ or $\text{Bi}_2\text{A}_{m-1}\text{B}_m\text{O}_{3m+3}$, where the symbol m in said formula is a positive number, the symbol A is at least one element selected from Na, K, Pb, Ba, Sr, Ca, and Bi, and the symbol B is at least one element selected from Fe, Co, Cr, Ga, Ti, Nb, Ta, Sb, V, Mo, and W.

Takayuki teaches the use of a ferroelectric thin film body which can be used as a ferroelectric layer in an electronic component, wherein the dielectric film is comprised of a bismuth layer structured compound wherein the c axis is oriented substantially vertically with respect to the plane of a thin film forming substrate, and said bismuth layer structured compound is expressed by the following formula $(\text{Bi}_2\text{O}_2)^{2+}(\text{A}_{m-1}\text{B}_m\text{O}_{3m+3})^{2-}$ or $\text{Bi}_2\text{A}_{m-1}\text{B}_m\text{O}_{3m+3}$, where the symbol m in said formula is a positive number, the symbol A is at least one element selected from Na, K, Pb, Ba, Sr, Ca, and Bi, and the symbol B is at least one element selected from Fe, Co, Cr, Ti, Ta, and W (see claim 2).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the ferroelectric thin film body of Takayuki et al. in the decoupling capacitor of '305, since such a modification would form a capacitor with a bismuth layer structure compound insulator having a high dielectric constant.

Regarding claim 2, '305 discloses the capacitor is a decoupling capacitor connected in parallel between the power source and an integrated circuit.

Regarding claim 4, '305 discloses the capacitor is arranged near an integrated circuit chip.

Regarding claim 5, '305 discloses the capacitor is arranged in contact with an integrated circuit.

Regarding claim 11, '305 disclose the capacitor has a lower electrode formed on a thin film substrate, the dielectric thin film formed on said lower electrode, and an upper electrode formed on said dielectric thin film (see fig. 6).

Regarding claim 13, Takayuki teaches that the bismuth layer structure compound has a c axis orientation of at least 80%.

6. Claims 1, 2, 9, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takeshima et al. (JP 11-214245) in view of Iino et al. (US 6,370,013) and Takayuki (JP 08-253324).

Regarding claims 1, 2, 9, and 12, Takeshima et al. disclose a thin film monolithic capacitor comprising electrodes separated by dielectric layers.

Takeshima et al. disclose the claimed invention except that the capacitor functions as a decoupling capacitor within a printed circuit board, and the dielectric film being formed with a bismuth layer structured compound wherein the c axis is oriented substantially vertically with respect to the plane of a thin film forming substrate, and said bismuth layer structured compound is expressed by the following formula $(\text{Bi}_2\text{O}_2)^{2+}(\text{A}_{m-1}\text{B}_m\text{O}_{3m+3})^{2-}$ or $\text{Bi}_2\text{A}_{m-1}\text{B}_m\text{O}_{3m+3}$, where the symbol m in said formula is a positive number, the symbol A is at least one element selected from Na, K, Pb, Ba, Sr, Ca, and Bi, and the symbol B is at least one element selected from Fe, Co, Cr, Ga, Ti, Nb, Ta, Sb, V, Mo, and W.

Takayuki teaches the use of a ferroelectric thin film body which can be used as a ferroelectric layer in an electronic component, wherein the dielectric film is comprised of a bismuth layer structured compound wherein the c axis is oriented substantially vertically with respect to the plane of a thin film forming substrate, and said bismuth layer structured compound is expressed by the following formula $(\text{Bi}_2\text{O}_2)^{2+}(\text{A}_{m-1}\text{B}_m\text{O}_{3m+3})^{2-}$ or $\text{Bi}_2\text{A}_{m-1}\text{B}_m\text{O}_{3m+3}$, where the symbol m in said formula is a positive number,

the symbol A is at least one element selected from Na, K, Pb, Ba, Sr, Ca, and Bi, and the symbol B is at least one element selected from Fe, Co, Cr, Ti, Ta, and W (see claim 2).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the ferroelectric thin film body of Takayuki et al. in the capacitor of Takeshima et al., since such a modification would form a capacitor with a bismuth layer structure compound insulator having a high dielectric constant.

Iino et al. teach that it is known in the art to connect a monolithic thin film capacitor between a power source and an integrated circuit so as to reduce the power source noise.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the monolithic capacitor of Takeshima et al. in the printed circuit board of Iino et al., since such a modification would form a thin stacked type capacitor within a printed circuit board, wherein the thin stacked type capacitor having a high dielectric constant insulator.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Thomas whose telephone number is 571-272-1985. The examiner can normally be reached on Monday - Friday 5:30 AM - 2:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego Gutierrez can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2831

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

et

/Eric Thomas/
Primary Examiner, Art Unit 2831